CALL 2008

## Project profile

ENIAC JOINT UNDERTAKING

# LENS

## *Lithography process for beyond 32nm manufacturing*

The ENIAC JU LENS project will develop and integrate the overall infrastructure required to process 32 and 22nm technology semiconductor chip nodes through double patterning and pitch-doubling technology on existing conventional immersion-exposure lithographic tools. This should, in turn, allow for the timely development of 32 and 22nm technology nodes for memory circuits and logic devices and provide a satisfactory alternative to extreme ultra-violet (EUV) lithography, higher refraction index fluids for immersion lithography and maskless lithography, which all seem to be far from maturity.

### Sub Programme

- Equipment and Materials for Nanoelectronics

In the world of silicon-wafer fabrication, water-immersion lithography has been widely accepted as the standard patterning technology for the 45nm technology node but solutions for 32 and 22nm nodes are not yet clear. Extreme ultra-violet (EUV) lithography is not yet available for industrial use, in spite of impressive progress, and multiple electron-beam lithography is still in development.

Double patterning seems to be the only viable, cost-effective option for the development of future process generations within the time limits defined by the International Technology Roadmap for Semiconductors (ITRS).

The final objective of the ENIAC LENS project is to demonstrate 22nm node patterning on 1.35 numerical-aperture (NA) immersion tools with very complex mask sets. Resolution, alignment and line-width control should comply with the 2007 ITRS requirements for the corresponding technology nodes.

### *Many options*

Extending immersion lithography from the 45nm node down to 32 and 22nm would require higher refraction index liquids and new materials for lenses and resists. The development of lithography systems with numerical apertures higher then 1.35, the maximum value currently achievable with water immersion, is facing difficulties and has been delayed by most tool manufacturers.

Introduction of EUV would require radical changes to both process and mask technologies. Despite recent progress, the availability of EUV technology on time cannot be assumed and would anyway be expensive. In this uncertain context, double patterning allows lithography to go beyond the resolution capability of existing tools without drastic changes in manufacturing infrastructures or massive investments.

## Novel process development

LENS is therefore developing and validating a novel integrated double-patterning process for immersion lithography in line with 22nm technology node ITRS requirements. Although the introduction of double patterning will not require a complete change of the manufacturing infrastructure, several issues must be addressed to make this technology mature enough to support industrial production. Research and innovation are required across the whole supply chain.

The ENIAC JU project will assess critical issues related to both pitch-doubling and double-exposure double patterning in parallel, since it is not clear yet which will be the winner. Pitch doubling is simpler and could be probably used first to support prototype development, while double exposure looks more flexible but requires dedicated equipment development.

In double patterning, the critical-dimension (CD) difference between two lines is twice the overlay error; the best performance demonstrated so far has never been able to produce a minimum misalignment below 5nm. New exposure and metrology tools specifically optimised for double exposure, as well as sophisticated feedback control software, should improve that situation to allow overlay performance compatible with ITRS CD control specifications.

## Complete infrastructure

Extensive research effort is required in double-patterning process development and dedicated equipment meeting industrial requirements, both for the immersion stepper and the metrology equipment. Further software development is also required for process control, to link the two and to improve the performance limits of current equipment.

LENS intends to build the complete manufacturing infrastructure which will enable the selection of the right technology and its introduction in an industrial environment for the 32nm node, and an assessment of the feasibility for the 22nm node. The selected double-patterning approach will be demonstrated on the critical layers of test devices, fully representative of advanced logic and memory circuits of 32 and 22nm nodes.

Special attention will be put on the availability of the whole supply chain, including design, masks, exposure tools, materials, process flow and metrology, to support double-patterning technologies introduction in a production environment. Impact on design, yield and manufacturability issues will be addressed and a detailed cost-of-ownership analysis with respect to competing technologies will be carried out.

## Key enabling technology

By developing this critical technology step for the further evolution of nanoelectronics towards higher integration densities and lower costs, LENS will contribute to the successful implementation of several applications of major industrial and social importance. As such, it will act as key enabler for a large part of the ENIAC Joint Undertaking Multiannual Strategic Plan.

## Equipment and Materials

### Partners:
- ASML
- CEA-LETI
- Centro Nacional de Microelectrónica
- CIDETEC
- Dai Nippon Photomask Europe
- FEI Electron Optics
- IMEC
- JSR Micro
- LAM Research
- MENTOR Graphics
- Numonyx
- STMicroelectronics Crolles

### Project co-ordinator:
- Gerold Alberga, ASML

### Key project dates:
- Start: January 2009
- Finish: December 2011

### Countries involved:
- Belgium
- France
- Italy
- The Netherlands
- Spain

### Total budget:
- €30.56 million

The ENIAC Joint Undertaking, set up in February 2008, co-ordinates European nanoelectronics research activities through competitive calls for proposals. It takes public-private partnerships to the next level, bringing together the ENIAC member states, the European Commission and AENEAS, the association of R&D actors in this field, to foster growth and reinforce sustainable European competitiveness.

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