

## Project profile

# MODERN

## *Modelling and design of reliable, process variation-aware nanoelectronics devices, circuits and systems*



The objective of the MODERN project is to develop new paradigms in integrated-circuit design that will speed up the development and improve the manufacture of reliable, low-cost, low electromagnetic interference and high-yield complex products. Reducing the effect of process variations, ensuring electromagnetic compatibility and handling greater system complexity are the three major technical driving forces behind this ENIAC project. Solving such manufacturing difficulties will greatly advance the capabilities of European chipmakers and systems designers in the field of high technology worldwide.

### Sub Programme

- Design Methods and Tools for Nanoelectronics

The influence of process variations during the fabrication of semiconductor wafers for integrated circuits (ICs) is becoming critical for the nanometric CMOS technology nodes. This results from inherent geometric tolerances and manufacturing imperfections such as edge or surface roughness, or a fluctuation in the number of doping atoms. Consequently, production yields are inadequate.

Some level of variability has always existed and has been taken into account in design. However, for nanometric dimensions, the larger impact of variability and the greater influence of random or spatial imprecision pose a new challenge for device miniaturisation.

The main goals of the ENIAC

MODERN project, therefore, are:

- Advanced, yet accurate models of process variations for nanometric devices, circuits and complex architectures;
- Effective methods for evaluating the impact of process variations on manufacturability, design reliability and circuit performance in

terms of reliability, noise and electromagnetic interference (EMI), as well as timing, power and yield;

- Design methods and tools to mitigate or tolerate the effects of process variations at device, circuit and architectural levels; and
- Validation of modelling and design methods and tools on a variety of silicon demonstrators.

### **Process variations**

An often-neglected downside of technology scaling is the increased impact of geometric tolerances. In addition, when dealing with nanometric dimensions, edge and surface roughness or a fluctuation of the number of doping atoms within the channels become very significant. As a result, performance and power have become extremely sensitive to uncontrollable process variations.

Variations in a circuit parameter can be caused by environmental factors – such as power supply or temperature fluctuations – in operation and are typically transitory. Alternatively,

they may arise from physical factors in manufacturing that result in device or interconnect variations causing random or spatial deviations from design parameter values.

While process engineers have traditionally coped with die-to-die fluctuations, within-die variations are more subtle since they imply that different areas of the same die exhibit different values of the various parameters.

## Understanding EMI

Today's electronic circuits are truly heterogeneous system-on-chip (SoC) designs involving static random-access, read-only and embedded non-volatile memory and input/output drivers as well as digital and analogue circuitry integrated on the same die. Because of high-frequency square-waves rich in harmonics, plus an increasing level of power-rail noise, ICs are becoming prolific EMI generators and may have a significant detrimental impact on the overall reliability of electronic systems.

Until recently, circuit and package designers did not give much consideration to EMI. Reducing on-chip EMI has been more an art than a science; different engineering solutions were considered, tested and put into practice by trial and error, with no structured design methodology. This is no longer acceptable because international standards and regulations, customer requirements and aggressive competition dictate a deeper theoretical understanding.

In MODERN, new design methodologies, together with architectural solutions based on asynchronous and desynchronisation techniques, will

be defined and developed to provide product designers with an effective approach to reduce EMI. At the same time, this will satisfy the traditional constraints and mitigate the impact of process variability in order to fabricate more reliable and robust electronic systems.

## Complex systems

State-of-the-art silicon technologies such as those addressed in MODERN allow for very complex designs. Massively parallel processing solutions will tend to address a much larger part of application needs. This trend is similar to the progressive replacement of analogue processing by digital processing.

These parallel architectures are an opportunity to address process-variation issues. Industries involved in systems development have experience with complex architectures at both system equipment and SoC levels – such as radar-processing systems and image-processing chips. This type of experience is useful in applications with either real-time or safety-critical constraints.

## European advantage

The MODERN consortium features considerable competence and expertise in the field of advanced technologies, with a well-balanced participation between industry and research institutes. It brings together major design and manufacturing specialists from the European semiconductor domain who are collaborating to address fabrication issues that are in urgent need of resolution.

## Design Methods and Tools

### Partners:

- Alma Mater Studiorum – Università di Bologna
- austriamicrosystems
- CEA-LETI
- Centre Suisse d'Electronique et Microtechnologie (CSEM)
- Delft University of Technology
- Eindhoven University of Technology
- Elastic Clocks
- Graz University of Technology
- IMEP-LAHC Laboratory
- Infineon Technologies Austria
- Integrated System Development
- Italian University NanoElectronics Team (IUNET)
- Montpellier Laboratory of Computer Science, Robotics and Micro-electronics (LIRM)
- Numonyx Italy
- NXP Semiconductors Netherlands
- Politecnico di Torino
- Sapienza Università di Roma
- STMicroelectronics Crolles
- STMicroelectronics France
- STMicroelectronics Italy
- Synopsys Switzerland
- TEKLATECH
- Thales
- TIEMPO
- Universitat Politecnica de Catalunya
- University of Calabria
- University of Glasgow
- Vienna University of Technology

### Project co-ordinator:

- Jan C.H. van Gerwen, NXP Semiconductors

### Key project dates:

- Start: March 2009
- Finish: February 2012

### Countries involved:

- Austria
- Denmark
- France
- Greece
- Italy
- The Netherlands
- Spain
- Switzerland
- United Kingdom

### Total budget:

- €25.98 million



The ENIAC Joint Undertaking, set up in February 2008, co-ordinates European nanoelectronics research activities through competitive calls for proposals. It takes public-private partnerships to the next level, bringing together the ENIAC member states, the European Commission and AENEAS, the association of R&D actors in this field, to foster growth and reinforce sustainable European competitiveness.