CALL 2008

Project profile

eniac JOINT UNDERTAKING

IMPROVE

Implementing manufacturing science solutions to increase equipment productivity and fab performance

The European nanoelectronics industry must address both high volume manufacturing, for example for memories, and fabrication of a large variety of smaller volume complex products, such as mixed-signal chips, in an intensely competitive global environment, under the constraint to produce high-quality nanoscale devices at reasonable cost. The key objective of IMPROVE is to develop solutions that improve process quality and the effectiveness of production equipment – taking into account that the ownership cost of the equipment is the main contributor to the overall silicon-chip manufacturing cost.

Sub Programme

- Equipment and Materials for Nanoelectronics

Process control in semiconductor manufacturing is achieved through extensive use of metrology steps that measure critical dimensions, such as the length of the transistor gate, as well as scanning the surface to determine the number of defects created by contamination. There is a trade-off between the sampling needed to keep the process under control with high yields, and improving cycle time by reducing the number of wafers sampled.

It is not possible to verify that every transistor on every wafer is within the process window because of the huge number of transistors on a modern chip and the dramatic impact of extra metrology on cost and cycle time. Controlling process equipment for the next generation of technologies is a massive challenge for chipmakers.

The ENIAC IMPROVE project aims to increase the competitiveness of European semiconductor manufacturers by developing effective solutions to tighten the control of process variability while enhancing the reliability and productivity of manufacturing equipment. Advanced alternative techniques and algorithms will be evaluated at different fabrication sites.

Virtual metrology

The concept of virtual metrology is rapidly emerging as a technique which goes further than advanced equipment control and fault detection and classification and could alleviate the dependence on metrology steps. The principle behind virtual metrology is the prediction of metrology measurements from process parameters and processing equipment sensor data.

Virtual metrology appears to be the only way to reach the required level of control. This type of prediction will allow the measurement of virtually all processed wafers, thus improving device quality and yield. It will also enable reduced sampling at standard metrology steps. It will, therefore, contribute to the reduction of variability and cycle time by the elimination of non-value-added steps.

Equipment effectiveness

Considering the huge amount of capital expenditure represented by the process tools in a leading edge semiconductor fabrication facility, it is absolutely critical to maximise the use of these assets. The current availability and reliability of semiconductor production tools can and must be improved.

Equipment use must be optimised, not only in terms of throughput – process speed – and quality of result supporting the improvement in process stability and reproducibility, but also with regard to overall efficiency, simply measured by the total number of hours equipment is up and running within a certain normalised timeframe. This becomes even more important for equipment on lines that have a high mix of products and technologies to be processed.

Art of prediction

One task will be to develop a predictive equipment-behaviour system. The prediction of equipment behaviour will anticipate failures and launch ad-hoc preventive maintenance actions. Specifying a predictive-maintenance strategy will improve cycle time and yield by reducing unscheduled equipment downtime and wafer scrap.

Both virtual metrology and predictive maintenance rely on intensive modelling activities using similar inputs – namely the equipment parameters. They will therefore interact and that is why it makes sense to study the two subjects in the same project.

The concept of dynamic risk assessment will make it possible to benefit from virtual metrology and predictive-equipment behaviour. It will allow dynamic adaption of the control plan, decreasing the number and frequency of controls in stable areas while increasing them in more unstable areas.

In addition, IMPROVE will focus on the essential enablers of predictive equipment control and virtual-metrology solutions, such as factory information and control systems (FICS). Implementation of new methods on a production line requires their integration with the decision system in the factory together with the development of a dedicated FICS. The development of existing systems plus prototyping and testing of such FICS developments will also be analysed.

Boosting productivity

The IMPROVE project will enable the development of the tools and methods needed to implement virtual metrology and predictive equipment-behaviour systems, the use of these results to optimise the control plan dynamically and to integrate them with the FICS. The ability to reduce unscheduled equipment downtime, metrology effort and wafer scrap on the production lines of the project partners will also have been assessed.

A major outcome will be the encouragement of European chipmakers to move from reactive to predictive factory operations to increase equipment productivity and the performance of their wafer-fabrication facilities.

Equipment and Materials

Partners:

- austriamicrosystems
- Camline
- CEA-LETI
- Critical Manufacturing
- Dublin City University
- Ecole des Mines de Saint Etiennes – Centre Microélectronique de Provence
- Fachhochschule Wiener Neustadt
- FAU Erlangen-Nürnberg
- Fraunhofer-Gesellschaft
- G-SCOP
- Infineon Austria
- Infineon Dresden
- Infineon Technologies
- InReCon
- Intel
- iSyst Intelligente Systeme
- Italian National Research Council (CNR)
- LAM Italy
- LAM Research Ireland
- Lexas Research
- LFoundry Rousset
- LTM CNRS
- Numonyx
- PDF solutions
- Probayes
- STMicroelectronics Crolles
- STMicroelectronics Italy
- STMicroelectronics Rousset
- Techno Fittings
- University of Augsburg
- University of Milan
- University of Padua
- University of Pavia

Project co-ordinator:

- François Finck, STMicroelectronics

Key project dates:

- Start: March 2009
- Finish: February 2012

Countries involved:

- Austria
- France
- Germany
- Ireland
- Italy
- Portugal

Total budget:

- €37.61 million

The ENIAC Joint Undertaking, set up in February 2008, co-ordinates European nanoelectronics research activities through competitive calls for proposals. It takes public-private partnerships to the next level, bringing together the ENIAC member states, the European Commission and AENEAS, the association of R&D actors in this field, to foster growth and reinforce sustainable European competitiveness.

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